REMARKS

Claims 1-27 remain in the application.

Claim Rejections under 35 U.S.C. § 102(b)

Claims 1-5, 11, 17-19 and 25-27 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,161,166 to Doing et al. ("Doing").

Embodiments of the present invention pertain to reducing a size of a linear address of an instruction. Using the full linear address to access an array, such as a tag array results in the tag array storing addresses having the same size as the full linear address. By reducing the size of the linear address, the size of the tag array may be reduced as well.

In one example shown in Figure 1, a reduction module 46 in an instruction translation look-aside buffer (ITLB) 18 receives full linear addresses from the processor bus 24 and converts these addresses into reduced linear addresses. In the example of Figure 1, a full linear address has a size of 32 bits and the reduced linear address has a size of 23 bits.

Doing describes an instruction cache for a multithreaded processor. There are several addresses described in Doing (and shown in Figure 8). An effective address is 64 bits in size. The highest order bits (36 bits) are used as a lookup value in a segment table 821 to produce a 52-bit value that is concatenated onto the lower 28 bits of the effective address. This is a virtual address and is 80 bits in size. The highest order bits (68 bits) of the virtual address are used as a lookup value in a page table 822 to produce a 28-bit value that is concatenated onto the lower 12 bits of the virtual address. This is the read address and is 40 bits in size.

Looking at Figure 4A of Doing, seven bits of the 64-bit effective address are input into a hash select component (select logic 401). As indicated at Col. 10, lines 26-36, the select logic takes the following as inputs: the seven bits of the effective address (i.e., EA_{45} to EA_{51}); a multi-thread control line (MT); and an active thread line (ActT). The hash function is taking the seven bits of the effective address along with the MT and ActT signals and producing a seven-bit value to be used to look up a value in the ERAT 301 (effective-to-read address table). As indicated by the equation at lines 34 and 35, the result of this function is labeled $HASH_{0:6}$. Given the description at lines 26-33 of Col. 10 and what is shown in Fig. 4A, it is believed that references to EA_{38} and EA_{39} in the equation on lines 34-35 Col. 10 are typographical errors and should be EA_{48} and EA_{49}, respectively.

Claim 1, for example, recites that a full linear address of an instruction is received and reduced in size to obtain a reduced linear address. According to the Office Action, the effective address in Doing is converted into a seven bit value using the described hash function. As described above, no reduction in the size of the effective address is performed at all in Doing. Seven bits of the effective address are received and converted into seven bits as the output of the hash function. Since no reduction in size of the effective address occurs in Doing, this reference fails to teach this feature of claim 1. A similar argument applies to claims 11, 17 and 25 as well.

Claim 2, for example, recites hashing a subset of the full linear address to reduce the size of the full linear address. Though a hashing function is described in Doing, that function does not hash a subset of the full linear address to reduce the size of the full linear address as called for in this claim. A similar argument applies to claims 11, 18, and 26.

Since features of the independent claims 1, 11, 17, and 25 are neither taught nor suggested by Going, reconsideration and withdrawal of the rejection of these claims as well as dependent claims 2-5, 28-19 and 26-27 under 35 U.S.C. § 102(b) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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